AMENDMENTS TO THE DRAWINGS

The attached replacement sheet includes changes to Figure 1, which is now labeled as "Prior Art".

REMARKS

Claims 1-19 have been examined, with claims 1-16 and 19 rejected. Applicants appreciatively acknowledge the Examiner's indication of allowable subject matter in claims 17 and 18 and have placed these claims in condition for allowance by amending claim 17 to independent form. Applicants have also added new claim 20. Since this claim depends on claim 17, Applicants submit that it is patentable by virtue of its dependence on claim 17.

Invention Overview:

The present invention is directed to a circuit arrangement comprised of a first semiconductor chip configured to generate and transmit load control and pilot data to a second semiconductor chip. (See paragraphs 0054-0056 of the published application) Moreover, the second semiconductor chip is configured to drive electrical loads on the basis of a timing that is defined by the load control data. (See paragraph 0054 of the published application) The second semiconductor chip is further configured to transmit diagnostic data to the first semiconductor chip and to control the transmission rate of the diagnostic data as prescribed by the pilot data transmitted by the first semiconductor chip. (See paragraphs 0034 & 0056-0057 of the published application)

Priority

The Examiner has indicated that Applicants have not filed a certified copy of the 02026774.6 application as required by 35 U.S.C. § 119(b). Applicants, however, submit that the priority document was filed as indicated by the filing receipt dated July 6, 2004.

Drawings

Figure 1 has been objected to as not being properly labeled. In response, Applicants submit herewith Figure 1 labeled as "Prior Art". Withdrawal of this objection is therefore respectfully requested.

Claim Rejections – 35 U.S.C. § 103(a)

Claims 1-16 and 19 have been rejected for the following prior art rejections:

1) Claims 1-4, 9-16 and 19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Arslain et al. (U.S. Patent No. 6,366,153) in view of Applicant Admitted Prior Art;[1]

2) Claims 5-7 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Arslain in view of Applicant Admitted Prior Art and Hastings et al. (U.S. Patent No. 6,772,251); and

3) Claim 8 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Arslain in view of Applicant Admitted Prior Art and Jeong (U.S. Patent No. 5,675,584).

Claim 1 is independent and claims 2-16 and 19 depend on claim 1. Applicants respectfully traverse these rejections for the reasons set forth below.

Independent Claim 1:

Independent claim 1 is directed to "An arrangement comprising ... a second semiconductor chip coupled to the first semiconductor chip ... wherein the second semiconductor chip is configured to ... c) control a transmission rate of the diagnostic data as prescribed by the pilot data." Neither Arslain nor the Admitted Prior Art disclose this element.

As acknowledged on page 3 of the Office Action, Arslain does not disclose the "transmission of the load control data and pilot data and that the second semiconductor chip transmits the diagnostic data." The Admitted Prior Art fails to make up for Arslain's deficiency.

[1] The Office Action incorrectly states on page 3 that claims 1-4 and 9-19 are rejected as being unpatentable over Arslain in view of the Admitted Prior Art. However, it is clear that claims 17 and 18 are not rejected for prior art reasons since the Examiner indicated on page 10 of the Office Action that these claims contain allowable subject matter.

Referring to Figure 1, the Admitted Prior Art discloses a microcontroller MC with three data lines DATA1*a*, DATA1*b* and DATA2 and two clock signal lines CLK1 and CLK2, all of which are coupled to the power chip PC. Load control data is transmitted to the power chip PC on the line DATA2 serially in time with a transmission clock signal transmitted via the line CLK2. (See paragraph 0025 of the published application.) Moreover, the microcontroller MC transmits pilot data on line DATA1*a* to the power chip PC serially in time with the transmission clock signal transmitted via the line CLK1. (See paragraph 0028 of the published application.) Synchronously, the power chip PC transmits diagnostic data to the microcontroller MC via line DATA1*b*, where such data is also sent serially in time with the transmission clock signal transmitted via the line CLK1. (See paragraph 0028 of the published application.) As such, transmission of diagnostic data in the Admitted Prior Art is dependent on the clock signal received from microcontroller MC.

In contrast, claim 1 requires that the power chip (*i.e.*, the second semiconductor chip) is configured to control a transmission rate of the diagnostic data as prescribed by the pilot data. The transmission of diagnostic data is, therefore, not dependent on a clock signal received from a first semiconductor chip. Advantageously, this configuration obviates the need to transmit a clock signal from the first semiconductor chip to the second semiconductor chip. (See paragraph 0035 of the published application.) Thus, independent claim 1, along with its dependent claims, is patentable over the applied references for at least this reason.

Dependent Claim 4:

Dependent claim 4, which depends on claim 1, further recites "wherein the diagnostic data are transmitted in time with a transmission clock signal generated in the second semiconductor chip, and the transmission clock signal is not transmitted to the first semiconductor chip."

The Office Action asserts that the Admitted Prior Art discloses this element citing the multiple "DATA" and "CLK" signals shown in Figure 1. However, the Admitted Prior Art discloses that clock signals are generated in the microcontroller MC (*i.e.*, the first semiconductor chip), not the second semiconductor chip, and are then transmitted to the power chip PC via lines

CLK1 and CLK2. (See paragraphs 0024 & 0027 of the published application.) Moreover, as discussed above, diagnostic signals are transmitted to the microcontroller MC serially in time with the transmission clock signal transmitted via the line CLK1. (See paragraph 0028 of the published application.) Thus, dependent claim 4 is also patentable over the applied prior art for this additional reason.

Dependent Claims 5-8:

Regarding claims 5-8, which all depend on claim 1, the applied references fail to make up for the deficiencies of Arslain and the Admitted Prior Art. Thus, these claims are patentable by virtue of their dependence on independent claim 1 as discussed above.

Conclusion

In view of the above remarks and amendments, Applicants believe the pending application is in condition for allowance.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

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Respectfully submitted,

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